INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
Agere Yee 7	~~TBA~~ 10/748,068
Applicant(s)	
Oceager P. Lee	
Filing Date	**Group Art Unit**
~~TBA~~ 12/29/2003	~~TBA~~ 2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JSR	A	6,249,893 B1	6/19/2001	Rajsuman et al.	714	741	
JSR	B	6,484,280 B1	11/19/2002	Moberly	714	726	
JSR	C	6,519,711 B1	2/11/2003	Fischer et al.	714	30	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

EXAMINER	DATE CONSIDERED
James Yun	10-5-05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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JUN 16 2005
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INFORMATION DISCLOSURE CITATION

(use several sheets if necessary)

Docket Number (Optional)	Application Number
6002-104US	10/748,068
Applicant(s)	
Oceager P. Yee	
Filing Date	**Group Art Unit**
12/29/2003	2825

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JGL		5,678,003	10/14/97	Jeffrey S. Brooks	714	34	
JGL		5,812,562	09/22/98	Sanghyeon Baeg	714	726	
JGL		6,385,742 B1	05/07/02	Graham Kirsch, et al.	714	39	
JGL		2002/0138801 A1	09/26/02	Laung-Terng Wang, et al.	714	729	

FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO
JGL		GB 2 337 834 A	01.12.1999	GB	—	—	✓	
JGL		WO 03/065065 A1	07.08.2003		—	—	✓	

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

JGL	1	"Silicon Debug: Scan Chains Alone Are Not Enough" by Gert Jan van Rootselaar and Bart Vermeulen; ITC International Test Conference; 1999 IEEE, pages 892-902
JGL	2	"Hierarchical Data Invalidation Analysis for Scan-Based Debug on Multiple-Clock System Chips" by Sandeep Kumar Goel and Bart Vermeulen; ITC International Test Conference; 2002 IEEE, pages 1103-1110

EXAMINER	DATE CONSIDERED
James Sun	10-5-05

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Filing Date	**Group Art Unit**
12/29/2003	2825

*EXAMINER INITIAL		OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
JSL	3	"Test and Debug Techniques for Multiple Clock Domain SoC Devices" by Ross R. Youngblood, Electronics Manufacturing Technology Symposium, 2004 IEEE, pages 202-205

EXAMINER	DATE CONSIDERED
James Lin	10-5-05

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